REMARKS/ARGUMENTS

Reconsideration and withdrawal of the rejections of the application are respectfully requested in view of the amendments and remarks herewith, which place the application into condition for allowance. The present amendment is being made to facilitate prosecution of the application.

I. STATUS OF THE CLAIMS AND FORMAL MATTERS

Claims 1-18 are currently pending. Claims 1, 6, 10, and 15 are independent. Claims 1, 2, 5, 6, 10, 11, 14 and 15 are hereby amended. No new matter has been introduced. Support for this amendment is provided throughout the Specification as originally filed. Changes to claims are not made for the purpose of patentability within the meaning of 35 U.S.C. §101, §102, §103, or §112. Rather, these changes are made simply for clarification and to round out the scope of protection to which Applicants are entitled.

II. REJECTIONS UNDER 35 U.S.C. §102(a)

Claims 1-18 were rejected under 35 U.S.C. §102(a) as allegedly unpatentable over U.S. Patent No. 5,977,997 to Vainsencher (hereinafter, merely "Vainsencher").

Claim 1 recites, *inter alia:*

> "A digital signal processing apparatus, comprising:
> ....
> a common bus for connecting said host arithmetic operation processing block and said plurality of digital signal processing blocks;

> interface means coupled to said common bus to enable a block to be added to the common bus or to enable a block connected to the common bus to be changed; and
>
> means for encrypting data of a stream transferred through said common bus." (emphasis added)

As understood by the Applicants, Vainsencher discloses three interfaces, the stream I/O interface, the primary memory interface, and the auxiliary memory interface. All three interface with physical entities or hardware such as the auxiliary memory, the primary memory, or a disk, etc. None of the interfaces of Vainsencher anticipate the interface means coupled to the common bus to enable a block to be added to the bus or to enable a block connected to the bus to be changed. Furthermore, the three interfaces that Vainsencher discloses are coupled to different busses. For example, in Vainsencher there are a main CPU bus for transmitting data and control signals between the CPU and the memory interface. The main CPU bus is separate from the at least one inter-processor bus, and a graphics bus operatively connecting the graphics rendering coprocessor and the memory interface. There is also provided a separate video bus operatively connecting the memory interface to the MPEG coprocessor and the display controller. As can be seen, Vainsencher discloses different interfaces interfacing with different busses.

Therefore, applicants respectfully submit that Vainsencher does not teach or suggest digital signal processing apparatus, comprising: a common bus for connecting said host arithmetic operation processing block and said plurality of digital signal processing blocks; interface means coupled to said common bus to enable a block to be added to the common bus or to enable a block connected to the common bus to be changed; and means for encrypting data of a stream transferred through said common bus, all as recited in claim 1.

For reasons similar to those described above with regard to independent claim 1, amended independent claims 6, 10, and 15 are also believed to be patentable.

Therefore, Applicants submit that independent claims 1, 6, 10, and 15 are patentably distinct over the cited references.

III. DEPENDENT CLAIMS

The other claims are dependent from the independent claim, discussed above, and are therefore believed patentable for at least the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

CONCLUSION

In the event the Examiner disagrees with any of statements appearing above with respect to the disclosure in the cited reference, it is respectfully requested that the Examiner specifically indicate those portions of the reference, providing the basis for a contrary view.

Please charge any additional fees that may be needed, and credit any overpayment, to our Deposit Account No. 50-0320.

In view of the foregoing amendments and remarks, it is believed that all of the claims in this application are patentable and Applicant respectfully requests early passage to issue of the present application.

Respectfully submitted,

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